

CLAIMS

1. A decoding method of decoding LDPC (Low Density Parity Check) codes, said decoding method comprising:

a decoding step of decoding said LDPC codes by using a
5 transformation check matrix obtained by performing one of or both a row permutation and a column permutation on an original check matrix.

2. The decoding method according to Claim 1, wherein, by using, as a formation matrix, a $P \times P$ unit matrix, a quasi-unit matrix in which one or more 1s, which are elements of the unit matrix, are substituted with 0, a shift matrix in which said unit matrix or said quasi-unit matrix is cyclically shifted, a sum matrix, which is the sum of two or more of said unit matrix, said quasi-unit matrix, and said 15 shift matrix, and a $P \times P$ 0-matrix, said transformation check matrix is represented by a combination of a plurality of said formation matrices.

3. The decoding method according to Claim 1, further comprising:

20 a code sequence permutation step of performing, on the code sequence of said received LDPC codes, the same column permutation as the column permutation performed on said original check matrix and outputting a permuted code sequence,

25 wherein, in said decoding step, said code sequence is

decoded by using said transformation check matrix and said permuted code sequence.

4. A decoding apparatus for decoding LDPC (Low Density Parity Check) codes, said decoding apparatus comprising:

5 decoding means for decoding said LDPC codes by using a transformation check matrix obtained by performing one of or both a row permutation and a column permutation on an original check matrix.

5. The decoding apparatus according to Claim 4, wherein, by
10 using, as a formation matrix, a $P \times P$ unit matrix, a quasi-unit matrix in which one or more 1s, which are elements of the unit matrix, are substituted with 0, a shift matrix in which said unit matrix or said quasi-unit matrix is cyclically shifted, a sum matrix, which is the sum of two or
15 more of said unit matrix, said quasi-unit matrix, and said shift matrix, and a $P \times P$ 0-matrix, said transformation check matrix is represented by a combination of a plurality of said formation matrices.

6. The decoding apparatus according to Claim 5, wherein
20 said decoding means comprises:

check node calculation means for simultaneously performing p check node computations for decoding said LDPC codes; and

variable node calculation means for simultaneously performing p variable node computations for decoding said

LDPC codes.

7. The decoding apparatus according to Claim 6, wherein said check node calculation means comprises p check node calculators for performing computations of check nodes, and

5 said variable node calculation means comprises p variable node calculators for performing computations of variable nodes.

8. The decoding apparatus according to Claim 6, wherein said decoding means further comprises message storage means
10 for simultaneously reading and writing message data corresponding to p edges obtained as a result of said computations of the p check nodes or the p variable nodes.

9. The decoding apparatus according to Claim 8, wherein said message storage means stores message data corresponding
15 to the edges which are read during a check node computation in such a manner that 1s of said transformation check matrices are padded closer in the row direction.

10. The decoding apparatus according to Claim 8, wherein said message storage means stores message data corresponding
20 to the edges which are read during a variable node computation in such a manner that 1s of said transformation check matrix is padded closer in the column direction.

11. The decoding apparatus according to Claim 8, wherein said message storage means stores, at the same address,
25 messages corresponding to p edges belonging to a unit matrix,

a quasi-unit matrix, or a shift matrix whose weight is 1 when the formation matrices, whose weight is 2 or more, representing said transformation check matrix are represented in the form of the sum of the unit matrix, the
5 quasi-unit matrix, or the shift matrix, whose weight is 1.

12. The decoding apparatus according to Claim 8, wherein said message storage means comprises number-of-the-rows/p FIFOs and number-of-the-columns/p FIFOs, and

10 said number-of-the-rows/p FIFOs and said number-of-the-
columns/p FIFOs each have a number of words corresponding to the weight of the rows and columns of said check matrix.

13. The decoding apparatus according to Claim 8, wherein said message storage means comprises a RAM (Random Access Memory), and

15 said RAM stores said message data in such a manner as to be padded closer in the read-out sequence and reads said message data in the storage position sequence.

14. The decoding apparatus according to Claim 6, wherein said decoding means further comprises received information
20 storage means for storing received information and simultaneously reading p pieces of the received information.

15. The decoding apparatus according to Claim 14, wherein said received information storage means stores said received information in such a manner that said received information
25 can be read in the sequence necessary for said computations

of variable nodes.

16. The decoding apparatus according to Claim 6, wherein
said decoding means further comprises cyclic shift means for
cyclically shifting messages obtained as a result of said p
5 check node computations or said p variable node computations.

17. The decoding apparatus according to Claim 16, wherein
said cyclic shift means comprises a barrel shifter.

18. The decoding apparatus according to Claim 4, further
comprising code sequence permutation means for performing,
10 on the code sequence of said received LDPC codes, the same
column permutation as the column permutation performed on
said original check matrix and outputting a permuted code
sequence,

wherein said decoding means decodes said code sequence
15 by using said transformation check matrix and said permuted
code sequence.

19. The decoding apparatus according to Claim 18, further
comprising inverse permutation means for performing, on the
output of said decoding means, an inverse permutation of a
20 column permutation performed on said original check matrix,
and for outputting a final decoded result.

20. A program for enabling a computer to decode LDPC (Low
Density Parity Check) codes, said program comprising:

a decoding step of decoding said LDPC codes by using a
25 transformation check matrix obtained by performing one of or

both a row permutation and a column permutation on an original check matrix.